VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please cancel claims 1, 7, 8, 15 and 16 without prejudice or disclaimer, and amend the claims remaining in the application as follows:

2. (Amended) A semiconductor device comprising:

a semiconductor chip,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer and connected to said electrodes, and

external terminals provided on said circuit layer, wherein

an organic protecting film is provided on the plane opposite to said stress relaxing layer of said semiconductor chip, and

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed outside of the semiconductor device on a same plane.

3. (Amended) A semiconductor device comprising:

a semiconductor chip,

a porous stress relaxing layer provided on a plane, whereon circuits

and electrodes of said semiconductor chip are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer,

via-holes provided between the electrodes on said semiconductor chip and said circuit layer,

conductive portions for connecting electrically said circuit layer and said electrodes in said via-holes,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the plane where the circuits and electrodes of said semiconductor chip are formed, wherein

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed outside of the semiconductor device on a same plane.

4. (Amended) A semiconductor device as claimed in [any one of claim 1 to claim 3] claim 2 or 3, wherein

said organic protecting film has a linear expansion coefficient equivalent to the linear expansion coefficient of said stress relaxing layer.

9. (Amended) A semiconductor device comprising:

a semiconductor chip,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes of said semiconductor chip are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer,

anisotropic conductive material for connecting electrically said circuit layer and said electrodes on said semiconductor chip,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the plane, where the circuits and electrodes of said semiconductor chip are formed, wherein

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed outside of said semiconductor device on a same plane.

10. (Twice Amended) A semiconductor wafer comprising:

a chip for forming a semiconductor device, having a plurality of chip areas comprising circuits and electrodes, respectively,

a porous stress relaxing layer provided on a plane of said chip,

whereon the circuits and the electrodes are formed,

a circuit layer provided on said stress relaxing layer, and connected to said electrodes, and

external terminals provided on said circuit layer, wherein

an organic protecting film is provided on the plane opposite to the plane, whereon said porous stress relaxing layer is provided, of said chip, and

side planes of the stress relaxing layer are exposed to outside of the semiconductor device.

11. (Twice Amended) A semiconductor wafer comprising:

a chip for forming a semiconductor device, having a plurality of chip areas comprising circuits and electrodes, respectively,

a porous stress relaxing layer provided on a plane of said chip, whereon the circuits and the electrodes of said chip area are formed,

a circuit layer provided on said stress relaxing layer,

via-holes provided between said electrodes and said circuit layer,

conductive portions for electrically connecting said circuit layer and said electrodes in said via-holes,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane, opposite to the

stress relaxing layer, of said chip,

wherein side planes of the stress relaxing layer are exposed to outside of the semiconductor device.

17. (Twice Amended) A semiconductor wafer comprising:

a chip for forming a semiconductor device, having a plurality of chip areas comprising circuits and electrodes, respectively,

a porous stress relaxing layer provided on a plane of said chip, whereon the circuits and the electrodes of said chip area are formed,

a circuit layer provided on said stress relaxing layer,

anisotropic conductive material for connecting electrically electrodes on a chip [are] and a circuit layer,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the plane, [wherein] whereon said circuits and electrodes are formed, of said chip,

wherein side planes of the stress relaxing layer are exposed to outside of the semiconductor device.

20. (Amended) A semiconductor module mounted with plurality of semiconductor devices as claimed in any one of claims [1 to 9] 2 to 6 and 9.